Gayatri Vidya Parishad College of Engineering for Women (Autonomous)

Madhurawada, Visakhapatnam

(Affiliated to Andhra University, Visakhapatnam)

I B.Tech. II Semester – Regular Examinations, June/ July – 2025

Subject Name: Digital Logic Design [24EC11RC05] **Max. Marks: 70 M**

Faculty Name : P V K Chaitanya **Branches: ECE, CSE, CSE(AIML), IT**

SCHEME OF VALUATION

Q No	Weightage	Total Marks
1 (a)	Decimal to hexadecimal ---------- 2M Decimal to octal ---------- 2M Binary to hexadecimal ---------- 1.5M Binary to octal ---------- 1.5M	7
1 (b)	Bit location Table ---------- 3M Parity bits generation ---------- 3M Hamming code with Parity bits ---------- 1M	7
2 (a)	For each subtraction Binary 2's complement representation ---------- 1.5M 2's complement subtraction ---------- 2M	7
2 (b)	BCD Representation ---------- 3M Excess-3 Representation ---------- 2M Excess-3 Representation ---------- 2M	7
3 (a)	Representation as product terms ---------- 2M Minimization using Boolean algebra ---------- 5M **or** Representing on K Map ---------- 2M Grouping the 1's ---------- 2M Product terms and Minimized expression ---------- 3M	7
3 (b)	Representing on K Map ---------- 2M Grouping the 1's ---------- 2M Product terms and Minimized expression ---------- 3M **or** Minimization using Boolean algebra ---------- 7M	7
4 (a)	NAND Realization ---------- 7M	7
4 (b)	Representing on K Map ---------- 1M Grouping the 1's ---------- 1M Product terms and Minimized expression ---------- 2M NAND Realization ---------- 3M	7
5 (a)	Combinational Logic Circuit definition ---------- 1M Full Adder Truth table and output expressions ---------- 3M Full Adder Implementation using Half adders ---------- 3M	7
5 (b)	Implementation of a BCD Adder using 4-bit adders ---------- 5M Explanation ---------- 2M	7

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6 (a)	Implementation of a 4-bit binary parallel adder/subtractor ---------- 5M Explanation ---------- 2M		**7**
6 (b)	2:4 Decoder using NAND gates ---------- 3M 2:4 Decoder using NOR gates ---------- 2M Explanation ---------- 2M		**7**
7 (a)	Conversion/ Excitation Table ---------- 3M K Map Simplification for S and R logic functions ---------- 2M Logic Diagram ---------- 2M		**7**
7 (b)	Implementation of a 4-bit bidirectional shift register ---------- 5M Explanation ---------- 2M		**7**
8	Drawback of JK Flipflop ---------- 2M Master-Slave JK Flipflop ---------- 5M		**7**
9	Excitation Table of counter ---------- 3M K Map Simplification ---------- 2M Logic Diagram of counter ---------- 2M		**7**
10 (a)	Design Explanation ---------- 3M State Diagram ---------- 4M		**7**
10 (b)	State Reduction definition ---------- 3M Advantages ---------- 4M		**7**

verified
(Dr. M. Mani kumari)

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