GAYATRI VIDYA PARISHAD COLLEGE OF ENGINEERING FOR WOMEN

(AUTONOMOUS)

(Affiliated to Andhra University, Visakhapatnam)

II B. Tech I Semester Regular Examinations, Nov- 2025

COMPUTER ORGANIZATION – 24CT11RC11

(Common to CSE, IT)

SCHEME OF VALUATION

Q. No.	Sub Q. No.	Scheme of Evaluation	Marks allotted
1.	a.	• Micro-operation • Three Types *1. Logical shift 2.Circular shift 3. Arithmetic shift*	1 2*3=6
1.	b.	• Definition of arithmetic shift & Convert to decimal (two's complement) • Perform Arithmetic Shift Right (ashr) & Convert to decimal • Detect Overflow Perform Arithmetic Shift Left (ashl)	3 2 2
2.	-	• Definition of Resister, RTL & Operations • Register Nomenclature • Solution for writing RTL Statements	5 3 2*3=6
3.	a.	• Timing Diagram and control unit explanation • Phases of Instruction Cycle & Flow Chart	3 4
3.	b.	• Format of instruction • Calculation of instructions encoding to memory references.	3 4
4.	-	• Different Instruction Codes • List and Explanation of memory, register, and I/O instructions	5 3*3=9
5.	a.	• Three-Address Instruction Format • Zero-Address Instruction Format	3 4
5.	b.	• Any 5 differences • Push &Pop operation	5 2
6.	a.	• Block Diagram • Explanation of Control Word	4 3
6.	b.	• Block Diagram • Explanation of Control Word	4 3
7.	-	• Phases of Instruction Cycle & Flow Chart • Timing Diagram • Pipeline Conflicts	5 5 4
8.	-	• Programmed I/O-Flowchart, advantages & Disadvantages. • Interrupt-Initiated I/O-Flowchart, advantages & Disadvantage. • DMA-Block Diagram, Working, advantages & Disadvantage.	4 4 6
9.	a.	• Required Hardware &Flowchart • Example	4 3
9.	b.	• No of chips & No of address Lines for 1024 bytes • No of chips & No of address Lines for 16K bytes	3 4
10.	a.	• Characteristics & Hierarchy diagram • System Performance	5 2
10.	b.	• Cache memory • Associative and two way Set-Associative mapping	3 2*2=4

Verified by

Prepared by,