Subject Code: 24EC11RC05 **R-24** **Reg No:**

GAYATRI VIDYA PARISHAD COLLEGE OF ENGINEERING FOR WOMEN

(AUTONOMOUS)

(Affiliated to Andhra University, Visakhapatnam)

I B.Tech. -II Semester Regular Examinations, June /July -2025

DIGITAL LOGIC DESIGN

(Common to ECE, CSE, CSE(AIML), IT)

1. All questions carry equal marks
2. Must answer all parts of the question at one place

Time : 3Hrs. **Max Marks: 70**

UNIT1

1. a. Convert given number in to Hexadecimal and octal forms

$(2365)_{10}$ and $(10101010101111)_2$ [7]

b. Given 8 bit data word 11110000, generate the 12 bit composite word for the even parity hamming code that corrects single errors. [7]

OR

2.a. Subtract the following numbers using 2s complement 28-78 and 128-456. [7]

b. Represent the following number 98457 in i) BCD II) EXCES-3 code iii) 5421 code. [7]

UNIT2

3.Obtain the simplified expression in sum of products for the following Boolean function.

a) F(A,B,C,D) = ∑(2,3,12,13,14,15). [7]

b) BDE + B'C'D + CDE + A'B'CE + A'B'C + B'C'D'E' [7]

OR

4. a. Draw the multiple level NAND circuit for the following expression: (AB'+CD')E + BC(A+B) [7]

b. Simplify the following four variable Boolean function and implement the same using NAND logic. F (A, B, C, D) = ∑ (0, 2, 4, 5, 6, 7, 8, 10, 13, 15) [7]

UNIT3

5.a. What is a combinational logic circuit? Implement a Full adder using two half adders and one OR gate. [7]

b) With a neat diagram explain in detail about BCD Adder. [7]

OR

6.a. Design and explain a 4-bit binary parallel Adder/Subtractor. [7]

b) Draw the logic diagram of 2:4 Decoder with an ENABLE input using: i) NAND gates ii) NOR gates. Show that the realization using NAND gates is more convenient to distinguish the selected output with a value of 0. [7]

UNIT4

7.a. Convert an SR Flip-Flop into JK Flip-Flop. [7]

b) With a neat diagram explain about 4-bit bidirectional shift register. [7]

OR

8. What is the drawback of JK flip flop, design a flip flop which overcomes this drawback and explain with neat diagram [14]

UNIT5

9.Design the counter that goes through states 1,2,4,5,7,8,10,11,1.....using JK flip-flops [14]

OR

10.a. Construct the state diagram of a sequence detector which detect 1100 with overlapping [7]

b. What is state reduction what are the advantages of state reduction. [7]