Subject Code: 24CT11RC11 **R-24** **Reg No:** | | | | | | | | | | | | |

GAYATRI VIDYA PARISHAD COLLEGE OF ENGINEERING FOR WOMEN

(Autonomous)

(Affiliated to Andhra University, Visakhapatnam)

II B.Tech. - I Semester Regular Examinations, Nov – 2025

Computer Organization

(Common to CSE & IT)

1. All questions carry equal marks
2. Must answer all parts of the question at one place

Time: 3Hrs. **Max Marks: 70**

UNIT-I

1	a)	Define micro-operation and explain the four Basic types of shift micro-operation and their variants.	7M
	b)	A computer uses a 16-bit register R that stores the signed binary number 1100110011001100. Determine the value of R in decimal after it undergoes an Arithmetic Shift Right operation. Also, state the condition under which an Arithmetic Shift Left operation causes an overflow.	7M

OR

2		Describe the function of Register Transfer Language (RTL). Write the RTL statements for the following operations: 1. The addition of the contents of registers R2 and R3, storing the result in R1. 2. A conditional transfer: If the input K=1, transfer the contents of R1 to R0.	14M

UNIT-II

3)	a)	Explain the function of the Timing and Control Unit in a basic computer. With a neat flowchart, explain the different phases that constitute the Instruction Cycle.	7M
	b)	A machine has 16-bit instruction codes. The Opcode is 4 bits. If there are 3 modes (Immediate, Direct, Indirect) and 4 general-purpose registers, determine the maximum number of Memory-Reference Instructions that can be defined	7M

OR

4)		Explain the concept of Instruction Codes (Memory-Reference, Register-Reference, and Input-Output instructions) and their structure in a basic computer.	14M

UNIT-III

5)	a)	Explain the influence of the number of addresses on computer program length. Illustrate this by writing the programs for the arithmetic statement X = (A+B) *(C+D) using Three-Address and Zero-Address instruction formats.	7M
	b)	Explain the concept of a Stack Organization in a CPU. Differentiate between a Register Stack and a Memory Stack, and detail the PUSH and POP operations	7M

OR

6	a)	With a neat block diagram, explain the General Register Organization of a CPU, focusing on how the common bus system and the decoder select the source and destination registers.	7M
	b)	Explain the Internal Architecture of the 8086 Microprocessor, focusing on the segregation into the Bus Interface Unit (BIU) and the Execution Unit (EU).	7M

UNIT-IV

7		Explain the concept of an Instruction Pipeline. Illustrate the speedup achieved using a four-stage pipeline. Discuss the three major types of pipeline conflicts (hazards) that cause the pipeline to stall.	14M

OR

8		Describe the three Modes of Transfer for communication between the CPU and I/O devices: Programmed I/O, Interrupt-Initiated I/O, and DMA. State the advantages and disadvantages of each.	14M

UNIT-V

9	a)	With an example, explain the step-by-step procedure of the Booth Multiplication Algorithm for multiplying two signed binary numbers.	7M
	b)	A computer uses RAM chips of 1024 x 1 capacity. a. How many chips are needed, and how should their address lines be connected to provide a memory capacity of 1024 bytes? b. How many chips are needed to provide a memory capacity of 16K bytes?	7M

OR

10	a)	Explain the three levels of the Memory Hierarchy in a computer system (Cache, Main Memory, Secondary Storage). Why is this hierarchy essential for system performance?	7M
	b)	Explain Cache with associative and two way Set-Associative mapping with a line size of 4 bytes	7M

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