UNIT-III

POWER ESTIMATION AND ANALYSIS

In VLSI design implementation simulation software operating at various levels of design abstraction. In general simulation at a lower-level design abstraction offers better accuracy at the expense of increased computer resource. Circuit simulators such as SPICE attain excellent accuracy but cannot be applied to full chip analysis. Logic simulation generally can handle full chip analysis but the accuracy is not as good and sometimes the execution speed is too slow. Behavioral level or functional level simulation offers rapid analysis but the accuracy is sacrificed.

The designer start with a simulation at the hardware behavior level to obtain an initial power dissipation estimate. When the gate gate-level design is available, a gate level simulation is performed to refine the initial estimate. If the initial estimate turns out to be inaccurate and the design fails the specification, the design is modified and verified again. The iteration continues until the gate level estimate is within specification. The design is then taken to the transistor or circuit level analysis to further verify the gate level estimates. The refinement and verification steps continue until the completion of the design process, when the chip is suitable for mass production.

SPICE Circuit Simulation

SPICE(Simulation Program with IC Emphasis) is the power analysis tool at the circuit level. SPICE operates by solving a large matrix of nodal current using the krichoff's current law(KCL).The basic components of SPICE are the primitive elements of circuit theory such as resistors, capacitors, inductors, current sources and voltage sources.More complex device models such as diodes and transistors constructed from the basic components.The device models are subsequently used to construct a circuit for simulation. Basic circuit parameters such as voltage, current, charge etc are reported by SPICE with high degree of precision. Hence the circuit power dissipation can be directly derived from SPICE simulation.

SPICE offers several analysis modes but the most useful mode for digital IC power analysis is called transient analysis. The analysis involves solving the DC solution of the circuit at time zero and makes small time increments to simulate the dynamic behavior of the circuit over time. Precise waveforms of the circuit parameters can be plotted over the simulation time. SPICE device models are derived from a characterization process. Each device model is described by dozens of parameters. The models are typically calibrated with physical measurements taken from actual test chips and can achieve a very high degree of accuracy. Low

power analysis tools using Finite Element Methods or other physical simulation can also be used to produce the device model parameters.

SPICE Power Analysis

SPICE can be used to estimate dynamic, static and leakage power dissipation.MOS and bipolar transistor models are typically available and it also faithfully captures many low level phenomena such as charge sharing, cross talk and transistor body effect. In addition it can handle common circuit components such as diodes, resistors, inductors and capacitors. Specialized components can often be built using the SPICE's modeling capability. SPICE analysis requires intensive computation resources and is thus not suitable for large circuits. Most SPICE-based simulators start to experience memory or computation limitation at several hundred to several thousand devices. Some advanced SPICE simulators can handle circuits up to ten thousand devices but simulating the entire chip is not possible. With the correct device models, SPICE simulations can reach accuracy within a few percent of physical measurement. The main source of error in SPICE is seldom found in the computation process but the inherent difficulties in modeling physical components and devices. Like any mass production process, the fabrication of semiconductor devices is subject to normal fluctuation and therefore SPICE's accuracy is often clouded by the variation of the chip production process. The most common method to cope with this problem is to apply extreme case analysis. Several sets of device models are generated to represent the typical and extreme conditions of the chip fabrication process and operating environment. The conditions are generally slowest operating extremes of the circuit. For example, most chip designers will simulate SPICE with three sets of parameters TYPICAL, BEST and WORST case conditions based on the device speed.

The variation of the semiconductor process could be large. The BEST and WORST case device speed could be 2X apart. The process variation of power dissipation is less but is still on the same order. For most circuits using conventional CMOS processes, faster device models generally correspond to higher power dissipation and vice-versa. However there are exceptions: for example, a low-speed worst case device model may cause slow signal slopes with high short-circuit power. For designs with marginal power budget, the analysis should be performed on some or all extreme cases to ensure specification compliance. The process variation problem affects all types of power and timing analysis using the bottom-up characterization approach. With SPICE, the problem is more severe due to the accuracy sought at this level of analysis.

Gate-level Logic Simulation

Simulation based gate level timing analysis has been a very mature technique in today's VLSI design. The component abstraction at this level is logic gates and nets. The circuit consists of components having defined logic behavior at its inputs and outputs such as NAND gates. Latches and Flip-Flops. Most gate level analysis can also handle capacitors and some can also handle resistors and restricted models of interconnect wires. Gate-level logic simulation software

is one of the earliest CAD tools being developed. Today, many gate-level logic simulators are available, most of which can perform full-chip simulation up to several million gates.

Basics of Gate-level Analysis

The most popular gate-level analysis is based on the so called event-driven logic simulation. Events are zero-one logic switching of nets in a circuit at a particular simulation time point. As one switching event occurs at the input of a logic gate, it may trigger other events at the output of the gate after a specified time delay. Computer simulation of such events provides a very accurate pre- fabrication logic analysis and verification of digital chips. Most gate level simulation also supports other logic states such as unknown, don't care and high impedance, to help the designer to simulate the circuit in a more realistic manner. Some simulators offer an extensive set of logic states for added accuracy in timing analysis. and VHDL are two popular languages used to describe gate level design. Recently, the cycle based simulators are being introduced into the design community. Such simulators assume that circuits are driven by master clock signals. Instead of scheduling events at arbitrary time points, certain nets of the circuit are only allowed a handful of events at a given clock cycle. This reduces the number of events to be simulated and results in more efficient analysis.

Many gate level simulators are so mature that special purpose computer hardware has been used to speed up the simulation algorithms. The idea is similar to the graphic processor in computer system. Instead of using a general purpose CPU to execute. This hardware acceleration technology generally results in several factors of speed up compared to using a general purpose computing system. Another technology that offers several orders of magnitude speedup in gate level analysis is called hardware emulation. Instead of simulating switching events using software programs, the logic network is partitioned into smaller manageable subblocks.The Boolean function of each sub-block is extracted and implemented with a connection network, carrying the logic signals, binds the sub-blocks together. Circuits up to a million gates can be emulated with this technology but this is also the most expensive type of logic simulator to operate and maintain because of the sophisticated high speed hardware required. The simulation speed is only one to two orders of magnitude slower than the actual VLSI chips to be fabricated. For example, a 200MHz CPU can be emulated with a 2MHz clock rate, permitting moderate real time simulation.

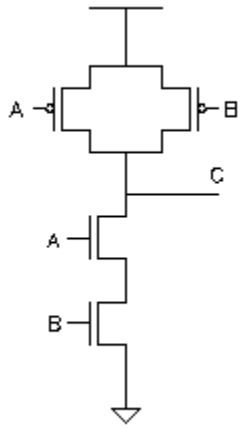
Capacitive Power Dissipation

Gate level power analysis based on logic simulation is one of the earliest power analysis tools developed. The basic principle of such tools is to perform a logic simulation of the gate level circuit to obtain the switching activity information. The information is then used to derive the power dissipation of the circuit. A major advantage of gate-level power analysis is that the $P=CV^2f$ equation can be computed precisely and easily. In a non-logic abstraction such as SPICE, the notion of the frequency of the node is not well defined because it has an analog

waveform that is potentially non periodic and non digital. In logic simulation, the switching activities of each node can be monitored to determine its frequency. The power dissipated due to charging and discharging capacitors can be easily computed. Each net i of a gate level circuit is associated with a capacitance C_i and a counter variable t_i.As simulation progresses ,a logic switching at net I increments the counter t_i. At the end of simulation, the frequency of net i is given by $f_i = t_{i/2T}$ where T is the simulation time elapsed. The capacitive power dissipation of the circuit is $P_{cap} = \sum_{net\ i} C_i V^2 f_i$. The simple gate-level power calculator is very useful in providing a quick estimate of the chip power dissipation.

Internal Switching Energy

The dynamic power dissipation inside the logic cell is called the internal power, which consists of short circuit power and charging or discharging of internal nodes. For a simple logic gate, the internal power consumed by the gate can be computed through a characterization process similar to that of timing analysis for logic gates. The idea is to simulate the "dynamic energy dissipation events" of the gate with SPICE or other lower-level power simulation tools. The computation of dynamic internal power uses the concept of logic events. Each gate has a pre-defined set of logic events in which a quantum of energy is consumed for each event. The energy value for each event can be computed with SPICE circuit simulation.



A 4 Transistor CMOS NAND gate

A	B	Y	Dyn energy (PJ)
1	r	f	1.67
1	f	r	1.39
r	1	f	1.94
f	1	r	1.72

Dynamic energy dissipation events

A	B	y	Static power (pW)
0	0	1	5.05
0	1	1	13.1
1	0	1	5.10
1	1	0	28.5

Static power dissipation states

For example a simple 4 transistor NAND gate has 4 dynamic energy dissipation events as shown in figure.The typical energy consumption of each event as shown in the table.This energy accounts for the short circuit current and charging and discharging of internal nodes of the gate.With the energy associated with each event ,we only need to know the occurrence frequency of each event from the logic simulation to compute the power dissipation associated with the event.The computation is repeated for all events of all gates in the circuit to obtain the total dynamic power dissipation as follows

$$P_{int} = \sum_{gate\ g} \sum_{event\ e} E(g,e) f(g,e)$$

In the above equation E(g,e) is the energy of the event e of gate g obtained from logic gate characterization and f(g,e) is the occurrence frequency of the event on the gate observed from logic simulation. The parameter E(g,e) depends on many factors like process conditions, operating voltage,temperature,output loading capacitance, input signal slopes.

The dynamic energy dissipation events not only depend on the Boolean function of the gate, but also the implementation of the gate.

Static State Power

The leakage power is primarily determined by the sub threshold and reverse biased leakage of MOS transistors. During logic simulation ,observe the gate for a period T and record

the fraction of time T(g,s)/T in which a gate g stays in a particular state s. Then perform this observation for all states of the gate to obtain the static leakage of the gate and repeat the computation for all gates to find the total static power dissipation as follows

$$P_{stat} = \sum_{gate\ g} \sum_{state\ s} P(g,s)T(g,s)/T$$

In the above equation P(g,s) is the static power dissipation of a gate g at state s obtained from characterization.The state duration T(g,s) is obtained from logic simulation. It is the total time the gate g stays at state s.The static power P(g,s) depends on process conditions, operating voltage, temperature etc.

Gate level capacitance Estimation

Capacitance is the most important physical attribute that affects the power dissipation impact on delays and signal slopes of logic gates. Changes in gate delays may affect the switching characteristics of the circuit and influence the power dissipation. Short circuit current is affected by the input signal slopes and output capacitance loading. Thus, capacitance has a direct and indirect impact on power analysis. The accurate estimation of capacitance is important for power analysis and optimization. Two types of parasitic capacitance exist in CMOS Circuits

1. Device parasitic capacitance 2. Wiring capacitance

The parasitic capacitance of MOS devices can be associated with their teriminals.The gate capacitance is heavily dependent on the oxide thickness of the gate that is process dependent. The design dependent factors are the width, length and shape of the gate. Typically, the shape of a transistor gate is rectangular and the width and length of the gate determine its capacitance. For a gate that “bends” eg:L shaped a correction factor can be used to find its equivalent rectangular width and length. The source and drain capacitance is also estimated from a similar method. The primary capacitance contribution of source and drain terminals is the area and shape of the diffusion regions. In general a larger transistor has more capacitance in all of its terminals.

In the cell based design environment, the design and layout of the library cells are made available before the chip design. The capacitance of each pin of a cell is therefore fixed by its circuit and layout. The pin capacitance of a cell can be accurately measured and stored in the cell library. One way to measure the pin capacitance is to use SPICE circuit simulation with the help of the capacitor I-V equation i=Cdv/dt we vary the pin voltage ΔV of the cell in time ΔT and observe the current I to obtain the capacitance c.This measurement can be performed during characterization of the cell.

The second source of parasitic capacitance is wiring capacitance.Wiring capacitance depends on the layer,area and shape of the wire.Typically the width of routing wires is set

to the minimum and the wiring capacitance is estimated from the lengths of the wires. In practice, the process dependent factors of wiring capacitance are expressed by a capacitance per unit length parameter that depends on the thickness of the wire, its dis stance from the substrate and its width. once the length of a wire is known, wiring capacitance can be computed. Wiring capacitance depends on the placement and routing of the gate level netlist, accurate estimation cannot be obtained before the physical design phase.However, there is still a need to perform capacitance estimation before physical design because the latter are lengthy processes. One way to solve this problem is to predict the wire length of a net from the number of pins incident to the net. This is called the wire load model in ASIC terms. A wire-load model provides a mapping of the nets pin-count to the wiring capacitance without actually knowing the exact length of the net. The mapping table can be constructed from historical data of existing designs. Sometimes, the function also depends on the number of cell of the circuit because the mapping of a ten thousand cell module and that of a one thousand cell module may be very different. Pre-layout wire-load model coupled with pin capacitance characterization can provide a good capacitance estimate for gate level power analysis. At the post lay out phase, when the actual lengths of the wires are known, the true wiring capacitance of a net can be used to verify the pre layout analysis.

Gate level Power Analysis

The event driven gate level power simulation is summarized as follows:

1. Run logic simulation with a set of input vectors.

2. Monitor the toggle count of each net, obtain capacitive power dissipation

3. Monitor the dynamic energy dissipation events of each gate, obtain internal switching power dissipation

4. Monitor the static power dissipation states of each gate. Obtain static power dissipation

5. Sum up all power dissipation components

The total power dissipation of the circuit is the sum of the three power components expressed in equation as $P= P_{cap}+P_{int}+P_{stat}$

The choice of simulation vectors needs to be considered carefully because power dissipation depends on them. The vectors should be chosen such that they reflect the desired operating conditions in which power analysis is sought. Generally the same vectors used for functional simulation and verification can be used for power analysis. The selection of simulation vectors is application dependent and should be determined from the operating environment of the chip. The vectors for test analysis are obviously not suitable for average power measurement because a chip does not normally operate in the test made.