II B.Tech (CSE)-CO-MCQs –Unit IV –I/O organization

1. In memory-mapped I/O _____ Ans:.(d)

a) The I/O devices have a separate address space
b) The memory and I/O devices have an associated address space
c) A part of the memory is specifically set aside for the I/O operation
d) The I/O devices and the memory share the same address space

2. The usual BUS structure used to connect the I/O devices is Ans.(c)
a) Star BUS structure b) Multiple BUS structure
c) Single BUS structure d) Node to Node BUS structure

3. The advantage of I/O mapped devices over memory mapped devices is Ans.(a)
a) The devices have to deal with fewer address lines
b)) The former offers faster transfer of data
c) The devices connected using I/O mapping have a bigger buffer space
d) No advantage as such

4. The system is notified of a read or write operation by---- -- Ans.(d)
a) Appending an extra bit of the address
b) Enabling the read/ write bit of the devices
c) Raising an appropriate interrupt signal d) Sending a special signal along the BUS

5. Use of ------takes care of the lag in the operating speeds of the I/O device and the processor Ans.(b)
a) BUFFERs b) Status flags c) Interrupt signals d) Exceptions

6. The method of accessing the I/O devices by repeatedly checking the status flags is

Ans.(a)

a) Program-controlled I/O b) Memory-mapped I/O c) I/O mapped d) DMA

7. The method of synchronising the processor with the I/O device in which the device sends a signal when it is ready is Ans.(c)
a) Exceptions b) Signal handling c) Interrupts d) DMA

8. The method which offers higher speeds of I/O transfers is ----- Ans.(c)
a) Interrupts b) Memory mapping c) Program-controlled I/O d) DMA

9. The process where in the processor constantly checks the status flags is called as---

Ans.(a)

a) Polling b) Inspection c) Reviewing d) Echoing

10 The interrupt-request line is a part of the-------- Ans.(c)
a) Data line b) Control line c) Address line d) None of the mentioned

11. The return address from the interrupt-service routine is stored on the---- Ans.(c)
a) System queue b) Processor register c) Processor stack d) Memory

12. The signal sent to the device from the processor after receiving an interrupt from it is

Ans.(a)
a) Interrupt-acknowledge b) Return signal c) Service signal d) Permission signal

13. When the process is returned after an interrupt service _____ should be loaded again.

Ans.(a)
i) Register contents ii) Condition codes iii) Stack contents iv) Return addresses
a) i,iv b) ii,iii and iv c) iii,iv d) i,ii

14. The time between the recieval of an interrupt and its service is _____ Ans.(b)
a) Interrupt delay b) Interrupt latency c) Cycle time d) Switching time

15. Interrupts form an important part of _____ systems. Ans.(c)

a) Batch processing b) Multitasking c) Real-time processing d) Multi-user

16. _____ type circuits are generally used for interrupt service lines Ans.(a) .
i) open-collector ii) open-drain iii) XOR iv) XNOR
a) i,ii b) ii c) ii,iii d) ii,iv

17. How can the processor ignore other interrupts when it is servicing one? Ans.(d)
a) By turning off the interrupt request line
b) By disabling the devices from sending the interrupts
c) BY using edge-triggered request lines d) All of the mentioned

18. When dealing with multiple device interrupts, which mechanism is easy to implement?

Ans.(a)
a) Polling method b) Vectored interrupts c) Interrupt nesting
d) None of the mentioned

19. The interrupt servicing mechanism in which the requesting device identifies itself to the processor to be serviced is _____ Ans.(b)
a) Polling b) Vectored interrupts c) Interrupt nesting d) Simultaneous requesting

20. In vectored interrupts, how does the device identify itself to the processor? Ans.(c)
a) By sending its device id b) By sending the machine code for the interrupt service routine
c) By sending the starting address of the service routine d) None of the mentioned

21. The code sent by the device in vectored interrupt is _____ long. Ans.(d)
a) upto 16 bits b) upto 32 bits c) upto 24 bits d) 4-8 bits

22. The starting address sent by the device in vectored interrupt is called as _____ Ans.(b)
a) Location id b) Interrupt vector c) Service location d) Service id

23. The processor invites to I/O devices to interrupt_____ Ans.(a)

a) By enabling the interrupt request line b) By enabling the IRQ bits
c) By activating the interrupt acknowledge line d) None of the mentioned

24. The processor indicates to the devices that it is ready to extend service ____ Ans.(c)
a) By enabling the interrupt request line b) By enabling the IRQ bits
c) By activating the interrupt acknowledge line d) None of the mentioned

25. Identify the form of communication best describes the I/O mode amongst the following:
a) Programmed mode of data transfer b) DMA Ans.(d)
c) Interrupt mode d) Polling

26. _____ method is used to establish priority by serially connecting all devices that request an interrupt. Ans.(b)
a) Vectored-interrupting b) Daisy chain c) Priority d) Polling

27. In daisy chaining device 0 will pass the signal only if it has _____ Ans.(b)
a) Interrupt request b) No interrupt request c) Interrupt request from device 1
d) no Interrupt request from device 1

28. _____ interrupt method uses register whose bits are set separately by interrupt signal for each device. Ans.(a)
a) Parallel priority interrupt b) Serial priority interrupt c) Daisy chaining d) None of the mentioned

29. ____ register is used for the purpose of controlling the status of each interrupt request in parallel priority interrupt. Ans.(d)
a) Mass b) Mark c) Make d) Mask

30. The ANDed output of the bits of the interrupt register and the mask register are set as input of: Ans.(b)
a) Priority decoder b) Priority encoder c) Process id encoder d) Multiplexer

31. If during the execution of an instruction an **exception** is raised then----- Ans.(b)
a) The instruction is executed and the exception is handled
b) The instruction is halted and the exception is handled
c) The processor completes the execution and saves the data and then handle the exception
d) None of the mentioned

32. _____ is/are types of exceptions. Ans.(d)
a) Trap b) Interrupt c) System calls d) All of the mentioned

33. The term ---- is used to refer to any event that causes an interrupt. Ans.(a)
a) Exception b) system call c) TRAP d) RST

34. The program used to find out errors is called---- -- Ans.(a)
a) Debugger b) Compiler c) Assembler d) Scanner

35. The two facilities provided by the debugger is ------ Ans.(c)
a) Trace and privileged points b) Privileged and Break points
c) Trace and break points d) none

36. In trace mode of operation, the program is ----- Ans.(a)
a) Interrupted after each detection of error
b) not stopped and the errors are sorted out after the complete program is scanned
c) executed without rectification of errors d) altered only at specific points

37. In Breakpoint mode of operation,the program is ---- Ans.(d)
a) interrupted after each detection of error
b) not be stopped and the errors are sorted out after the complete program is scanned
c) the program is executed without rectification of errors
d) The program is altered only at specific points

38. The different modes of operation of a computer is--- -Ans.(b)
a) User and System mode b) User and Supervisor mode
c) Supervisor and Trace mode d) Supervisor, User and Trace mode

39. The instructions which can be run only supervisor mode are----- Ans.(c)
a) Non-privileged instructions b) System instructions
c) Privileged instructions d) Exception instructions

40. A privilege exception is raised when a processor tries to ---------- Ans.(d)
a) change the mode of the system b) change the priority level of the other processes
c) access the memory allocated to other user d) All of the mentioned

41. How is a privilege exception dealt with? Ans.(a)
a) The program is altered and the system switches into supervisor mode and restarts the program execution
b) The Program is stopped and removed from the queue
c) The system switches the mode and starts the execution of a new process
d) The system switches mode and runs the debugger

42. The DMA differs from the interrupt mode by---- Ans.(c& d)
a) The involvement of the processor for the operation
b) The method accessing the I/O devices
c) The amount of data transfer possible
d) non intervention of CPU

43. The DMA transfers are performed by a control circuit called as---- Ans.(b)
a) Device interface b) DMA controller c) Data controller d) Overlooker

44.In DMA transfers, the required signals and addresses are given by the--- Ans.(c)
a) Processor b) Device drivers c) DMA controllers d) The program itself

45. After the complition of the DMA transfer the processor is notified by---- Ans.(b)
a) Acknowledge signal b) Interrupt signal c) WMFC signal d) None of the mentioned

46. The DMA controller has _____ registers Ans.(c)
a) 1 b) 2 c) 3 d) 4

47. When the R/W' bit of the status register of the DMA controller is set to 1, then Ans.(a)
a) Read operation is performed b) Write operation is performed
c) Read & Write operation is performed d) None of the mentioned

48. The DMA controller is connected to the ____ Ans.(b)
a) Memory BUS b) System BUS c) External BUS d) None of the mentioned

49 A DMA controller performs operations on two different disks simulteneously Ans.(a)
a) True b) False c) can not say d) some times True

50. The technique whereby the DMA controller steals the access cycles of the processor to operate is called---- Ans.(c)
a) Burst mode b) Transparent mode c) Cycle stealing d) hidden mode

51. The technique where the DMA controller is given complete access to main memory is---

Ans.(d)
a) Cycle stealing b) hidden mode c) transparent mode d) Burst mode

52. The DMA controller uses _____ to help with the transfers when handling network interfaces. Ans.(a)
a) Input Buffer storage b) Signal echancers c) Bridge circuits d) All of the mentioned

53. To overcome the conflict over the possession of the BUS we use _____ Ans.(b)
a) Optimizers b) BUS arbitrators c) Multiple BUS structure d) None of the mentioned

54. The registers of the DMA controller are _____ Ans.(c)
a) 64 bits b) 24 bits c) 32 bits d) 16 bits

55. When process requests for a DMA transfer ,THEN Ans.(d)
a) the process is temporarily suspended b) The process continues execution
c) Another process gets executed
d) process is temporarily suspended & Another process gets executed

56. The DMA transfer is initiated by _____ Ans.(b)
a) Processor b) The process being executed c) I/O devices d) OS

57. To resolve the clash over the access of the system BUS we use _____ Ans.(b)
a) Multiple BUS b) BUS arbitrator c) Priority access d) None of the mentioned

58. The device which is allowed to initiate DMA data transfers on the BUS at any time is called __ Ans.(a)
a) BUS master b) Processor c) BUS arbitrator d) Controller

59. _____ BUS arbitration approach uses the involvement of the processor Ans.(a)
a) Centralised arbitration b) Distributed arbitration c) Random arbitration
d) All of the mentioned

60. The circuit used for the BUS request line is a _____ Ans.(c)
a) Open-collector b) EX-OR circuit c) Open-drain d) Nand circuit

61. The Centralised BUS arbitration is similar to _____ interrupt circuit. Ans.(d)
a) Priority b) Parallel c) Single d) Daisy chain

62. When the processor receives the BUS request from a device, it responds by sending _____ Ans.(b)
a) Acknowledge signal b) BUS grant signal c) Response signal d) None of the mentioned

63. In Centralised Arbitration _____ is/are is the BUS master Ans.(d)
a) Processor b) DMA controller c) Device d) Both Processor and DMA controller

64. Once the BUS is granted to a device _____ Ans.(a)
a) It activates the BUS busy line b) Performs the required operation
c) Raises an interrupt d) All of the mentioned

65. The BUS busy line is made of _____ Ans.(b)
a) Open-drain circuit b) Open-collector circuit c) EX-Or circuit d) Nor circuit

66. The BUS busy line is used to indicate that the --------- Ans.(c)
a) processor is busy b) BUS master is busy
c) BUS is already allocated d) None of the mentioned

67. Distributed arbitration makes use of _____ Ans.(d)
a) BUS master b) Processor c) Arbitrator d) 4-bit ID

68. In Distributed arbitration, the device requesting the BUS _____
a) Asserts the Start arbitration signal b) Sends an interrupt signal
c) Sends an acknowledge signal d) None of the mentioned

69. How is a device selected in Distributed arbitration ? Ans.(c)
a) By NANDing the signals passed on all the 4 lines
b) By ANDing the signals passed on all the 4 lines
c) By ORing the signals passed on all the 4 lines d) None of the mentioned

70. If two devices A and B contesting for the BUS have ID's 5 and 6 respectively, which device gets the BUS based on the Distributed arbitration Ans.(b)
a) Device A b) Device B c) Insufficient information d) None of the mentioned

71. The primary function of the BUS is----- Ans.(a)
a) To connect the various devices to the CPU
b) To provide a path for communication between the processor and other devices
c) To facilitate data transfer between various devices d) All of the mentioned

72. The classification of BUSes into synchronous and asynchronous is based on--- Ans.(c)
a) The devices connected to them b) The type of data transfer
c) The Timing of data transfers d) None of the mentioned

73. The device which starts data transfer is called---- Ans.(d)
a) Master b) Transactor c) Distributor d) Initiator

74. The device which interacts with the initiator is------ Ans.(a)
a) Slave b) Master c) Responder d) initiator

75. In synchronous BUS, the devices get the timing signals from------- Ans.(b)
a) Timing generator in the device b) A common clock line
c) Timing signals are not used at all d) None of the mentioned

76. The delays caused in the switching of the timing signals is due to---- Ans.(c)
a) Memory access time b) WMFC c) Propagation delay d) Processor delay

77. The time for which the data is to be on the BUS is affected by------ Ans.(d)
a) Propagation delay of the circuit b) Setup time of the device
c) Memory access time d) Propagation delay of the circuit & Setup time of the device

78. The Master strobes the slave at the end of each clock cycle in Synchronous BUS.**True**.

79. What type of information is to be fed into the BUS first by the initiator..?? Ans.(d)
a) Data b) Address c) Commands or controls d) Address, Commands or controls

80. _____ signal is used as an acknowledgement signal by the slave in Multiple cycle transfers. Ans.(b)
a) Ack signal b) Slave ready signal c) Master ready signal d) Slave receive signal

81 The master indicates that the address is loaded onto the asynchronous, BUS by activating _____ signal. Ans.(a)
a) MSYN b) SSYN c) WMFC d) INTR

82. The devices with variable speeds are usually connected using asynchronous BUS.
Ans. True

83. The MSYN signal is initiated -------- Ans.(b)
a) Soon after the address and commands are loaded
b) Soon after the decoding of the address c) After the slave gets the commands
d) None of the mentioned

84. The BUS that allows I/O,memory and Processor to coexist is _____ Ans.(c)
a) Artibuted BUS b) Processor BUS c) Backplane BUS d) External BUS

85. The transmission on the asynchronous BUS is also called as _____ Ans.(d)
a) Switch mode transmission b) Variable transfer
c) Bulk transfer d) full Hand-Shake transmission

86. Asynchronous BUS mode of transmission is suitable for systems with multiple peripheral devices. Ans . True

87. The asynchronous BUS mode of transmission allows for a faster mode of data transfer.
Ans. False

88. _____ serves as a intermediary between the device and the BUSes.. Ans.(a)
a) Interface circuits b) Device drivers c) Buffers d) None of the mentioned

89. The side of the interface circuits, that has the data path and the control signals to transfer data between interface and device is _____ Ans.(b)
a) BUS side b) Port side c) Hardware side d) Software side

90. The interface circuits------ Ans.(c)
a) Helps in installing of the software driver for the device
b) Houses the buffer that helps in data transfer
c) Helps in decoding of the address on the address Bus d) None of the mentioned

91. The conversion from parallel to serial data transmission and vice versa takes place inside the interface circuits. Ans. True

92. The parallel mode of communication is not suitable for long devices because of ____ Ans.(a)
a) Timing skew b) Memory access delay c) Latency d) None of the mentioned

93. The Interface circuits generates the appropriate timing signals required by the BUS control scheme. Ans. True

94. The status flags required for data transfer is present in _____ Ans.(c)
a) Device b) Device driver c) Interface circuit d) None of the mentioned

95. The most popular input device used today for interactive processing ---- Ans.(a)
a) Mouse b) Magnetic disk c) Visual display terminal d) Card punch

96. The use of spooler programs or _____ Hardware allows PC operators to do the processing work at the same time a printing operation is in progress. Ans.(c)
a) Registers b) Memory c) Buffer d) CPU

97. _____ is used as an intermediate to extend the processor BUS. Ans.(a)
a) Bridge b) Router c) Connector d) Gateway

98. _____ is an extension of the processor BUS. Ans.(c)
a) SCSI BUS b) USB c) PCI BUS d) None of the mentioned

99. ISA stands for---- Ans.(b)
a) International American Standard b) Industry Standard Architecture
c) International Standard Architecture d) None of the mentioned

100. The video devices are connected to _____ BUS. . Ans.(d)
a) PCI b) USB c) HDMI d) SCSI

101SCSI stands for _____ Ans.(b)
a) Signal Computer System Interface b) Small Computer System Interface
c) Small Coding System Interface d) Signal Coding System Interface

102. The system developed by IBM with ISA architecture is _____ Ans.(c)
a) SPARC b) SUN-SPARC c) PC-AT d) None of the mentioned

103. IDE disk is connected to the PCI BUS using _____ interface. Ans.(a)
a) ISA b) ISO c) ANSI d) IEEE

104. IDE stands for _____ Ans.(a)
a) Intergrated Device Electronics b) International Device Encoding
c) Industrial Decoder Electronics d) International Decoder Encoder

105. The mode of transmission of data, where one bit is sent for each clock cycle is ____ Ans.(d)
a) Asynchronous b) Parallel c) Serial d) Isochronous

106. The transformation between the Parallel and serial ports is done with the help of ___ Ans.(c)
a) Flip flops b) Logic circuits c) Shift registers d) None of the mentioned

107. The serial port is used to connect basically _____ and processor. Ans.(a)
a) I/O devices b) Speakers c) Printer d) Monitor

108. The double buffer is used to ------- Ans.(a)
a) Enable to receive multiple bits of input b) Combine the input and output operations
c) Extend the buffer capacity d) None of the mentioned

109 UART stands for _____ Ans.(c)
a) Universal Asynchronous Relay Transmission b) Universal Accumulator Register Transfer
c) Universal Asynchronous Receiver Transmitter d) None of the mentioned

110. The key feature of UART is its ------ Ans.(d)
a) architectural design b) simple implementation c) general purpose usage
d) capability to connect to low speed devices also

111. The data transfer in UART is done in _____ Ans.(a)
a) Asynchronous start stop format b) Synchrnous start stop format
c) Isochronous format d) EBDIC format

112. The standard used in serial ports to facilitate communication is _____ Ans.(c)
a) RS-246 b) RS-LNK c) RS-232-C d) Both RS-246 and RS-LNK

113. In serial port interface, the INTR line is connected to _____ Ans.(b)
a) Shift register b) Status register c) Chip select d) None of the mentioned

114. The PCI bus follows a set of standards primarily used in _____ PC's. Ans.(c)
a) Intel b) Motorola c) IBM d) SUN

115. The _____ is the BUS used in Macintosh PC's. Ans.(a)
a) NuBUS b) EISA c) PCI d) None of the mentioned

116.One of the key features of the PCI BUS is-------- Ans.(b)
a) Low cost connectivity b) Plug and Play capability c) Expansion of Bandwidth
d) None of the mentioned

117. PCI stands for _____ Ans.(a)
a) Peripheral Component Interconnect b) Peripheral Computer Internet
c) Processor Computer Interconnect d) Processor Cable Interconnect

118. The PCI BUS supports _____ address space/s. Ans.(d)
a) I/O b) Memory c) Configuration d) All of the mentioned

119. _____ address space gives the PCI its plug and play capability.
a) Configuration b) I/O c) Memory d) All of the mentioned

120. _____ provides a separate physical connection to the memory. Ans.(a)
a) PCI BUS b) PCI interface c) PCI bridge d) Switch circuit

121. While transferring data over the PCI BUS, the master NEED NOT hold the address till the completion of transfer to the slave as The address is stored by the slave in a buffer. Ans. True

122. The master is also called as _____ in PCI terminology. Ans.(a)
a) Initiator b) Commander c) Chief d) Starter

123. Signals whose names end in ____ are asserted in the low voltage state. Ans.(b)
a) $ b) # c) * d) !

124. A complete operation over the BUS, involving the address and a burst of data is called ___

Ans.(a)

a) Transaction b) Transfer c) Move d) Procedure

125. The device connected to the PCI BUS is given an address of ____ bits during the initialisation phase. Ans.(b)

a) 24 b) 64 c) 32 d) 16

126. The PCI BUS has _____ interrupt request lines. Ans.(c)

a) 6 b) 1 c) 4 d) 3

127.In PCI bus ___signal is sent by the initiator to indicate the duration of the transaction. Ans.(a)

a) FRAME# b) IRDY# c) TMY# d) SELD#

128. In PCI bus _____ signal is used enable commands. Ans.(d)

a) FRAME# b) IRDY# c) TMY# d) c/BE#

129.In PCI Bus , the signal IRDY# is used for _____ Ans.(c)

a) Selecting the interrupt line b) Sending an interrupt c) Saying that the initiator is ready
d) None of the mentioned

130. In PCI Bus ,the following signal indicates that the slave is ready is _____ Ans.(b)

a) SLRY# b) TRDY# c) DSDY# d) None of the mentioned

131. In PCI Bus ,DEVSEL# signal is used----

a) To select the device b) To list all the devices connected Ans.(c)
c) By the device to indicate that it is ready for transaction d) None of the mentioned

132. In PCi Bus, the signal used to initiate device select _____ Ans.(d)

a) IRDY# b) S/BE c) DEVSEL# d) IDSEL#

133. The PCI BUS allows us to connect _____ I/O devices. Ans.(a)

a) 21 b) 13 c) 9 d) 11

134. The key features of the SCSI BUS is------- Ans.(b)

a) The cost effective connective media b) The ability overlap data transfer requests
c) The highly efficient data transmission d) None of the mentioned

135. In a data transfer operation involving SCSI BUS, the control is with _____ Ans.(b)

a) Initiator b) Target c) SCSI controller d) Target Controller

136. The SCSI bus signal DB(P) indicates that the data line is ------

a) carrying the device information b) carrying the parity information c) partly closed
d) temporarily occupied

137. The SCSI Bus signal **BSY** signifies that-------- Ans.(a)

a) The BUs is busy b) The controller is busy c) The Initiator is busy d) The Target is Busy

138. The SCSI Bus signal **SEL** signal signifies that the Ans.(b)

a) initiator is selected b) device for BUS control is selected
c) target is being selected d) None of the mentioned

139. The SCSI Bus signal that is asserted when the initiator wishes to send a message to the target. Ans.(b)
a) MSG b) APP c) SMS d) ATN

140. The SCSI Bus signal resets all the device controls to their startup state. Ans.(b)
a) SRT b) RST c) ATN d) None of the mentioned

141. The SCSI BUS uses _____ arbitration. Ans.(a)
a) Distributed b) Centralised c) Daisy chain d) Hybrid

142. SCSI stands for _____ Ans.(a)
a) Small Computer System Interface b) Switch Computer system Interface
c) Small Component System Interface d) None of the mentioned

143. A narrow SCSI BUS has _____ data lines. Ans.(b)
a) 6 b) 8 c) 16 d) 4

144. Single ended transmission means that all the signals have a ---- --- Ans.(c)
Ans.(c)
a) similar bit pattern b) common source
c) common ground return d) similar voltage signature

145. For better transfer rates on the SCSI BUS the length of the cable is limited to ____Ans.(d)
a) 2m b) 4m c) 1.3m d) 1.6m

146. The maximum number of devices that can be connected to SCSI BUS is _____ Ans.(c)
a) 12 b) 10 c) 16 d) 8

147, The SCSI BUS is connected to the processor through _____ Ans.(a)
a) SCSI Controller b) Bridge c) Switch d) None of the mentioned

148. The mode of data transfer used by the controller is _____ Ans.(b)
a) Interrupt b) DMA c) Asynchronous d) Synchronous

149. For SCSI bus communication with the disk drive ,the data is stored on the disk in the form of blocks is referred as _____ Ans.(c)
a) Pages b) Frames c) Sectors d) Tables

150. The transfer rate, when the USB is operating in low-speed of operation is ____ Ans.(d)
a) 5 Mb/s b) 12 Mb/s c) 2.5 Mb/s d) 1.5 Mb/s

151. The high speed mode of operation of the USB was introduced by _____ Ans.(c)
a) ISA b) USB 3.0 c) USB 2.0 d) ANSI

152. The USB supports the sampling process in speaker output to be a ____ process. Ans.(c)
a) Asynchronous b) Synchronous c) Isochronous d) None of the mentioned

153. The USB device follows _____ structure. Ans.(d)
a) List b) Huffmann c) Hash d) Tree

154. The I/O devices form the _____ of the tree structure.
a) Leaves b) Subordinate roots c) Left sub trees d) Right sub trees

155. USB is a serial mode of transmission of data. Ans .True.

156. USB allows only the host to communicate with the devices and not between themselves.
Ans. True.

157. The device can send a message to the host by taking part in _____ for the communication path . Ans.(b)
a) Arbitration b) Polling c) Prioritising d) None of the mentioned

158. When the USB is connected to a system, its root hub is connected to the _____ Ans.(c)
a) PCI BUS b) SCSI BUS c) Processor BUS d) IDE
159. The devices connected to USB is assigned an ____ address. Ans.(d)
a) 9 bit b) 16 bit c) 4 bit d) 7 bit 160.

160. The USB memory space is not under any address space and hence cannot be shared or accessed. Ans. True

161. Locations in the device to or from which data transfers can take place is called ___ Ans.(a)
a) End points b) Hosts c) Source d) None of the mentioned

162.USB pipe is a _____ channel. Ans.(c)
a) Simplex b) Half-Duplex c) Full-Duplex d) Both Simplex and Full-Duplex

163. The type/s of packets sent by the USB is/are _____ Ans.(d)
a) Data b) Address c) Control d) Both Data and Control

164. The first field of any packet to be transferred over the USB is _____ Ans.(a)
a) PID b) ADDR c) ENDP d) CRC16

165. The 4 bits PID's are transmitted twice, once with the true values and the second time with the complemented values.. Ans.True
166. The last field of any packet to be transferred over the USB is _____ Ans.(d)
a) PID b) ADDR c) ENDP d) CRC16

167. The CRC bits of the packet to be transferred over the USB are computed based on the values of the _____ Ans.(d)
a) PID b) ADDR c) ENDP d) Both ADDR and ENDP

168. The size of the data packets transmitted over USB can upto _____bytes. Ans.(c)
a) 512 b) 256 c) 1024 d) 2 KB

169. The most important objective of the USB is to provide _____ Ans.(d)
a) Isochronous transmission b) Plug and play c) Easy device connection d) All of the mentioned

170. The data transmission over the USB is divided into ____ Ans.(a)
a) Frames b) Pages c) Packets d) Tokens

171. The _____ signal is used to indiacate the beginning of a new frame. Ans.(b)
a) Start b) SOF c) BEG d) None of the mentioned

172. The signal SOF over USB transmission for every _____ Ans.(c)
a) 1s b) 5s c) 1ms d) 1Us

173. The power specification of usb is _____ Ans.(a)
a) 5v b) 10v c) 24v d) 10v