1. CPU fetches the instruction from memory according to the value of
   a**) program counter** b) status register
   c) instruction register d) program status word
2. Which one of the following is the address generated by CPU?
   a) physical address b) absolute address
   c) **logical address** d) none of the mentioned
3. Run time mapping from virtual to physical address is done by
   a) **Memory management unit** b) CPU
   c) PCI d) None of the mentioned
4. Memory management technique in which system stores and retrieves data from secondary storage for use in main memory is called
   a) fragmentation b**) paging**
   c) mapping d) none of the mentioned
5. Program always deals with
   a**) logical address** b) absolute address
   c) physical address d) relative address

Static Memories

6. The duration between the read and the mfc signal is _____
   a) Access time b) Latency
   c) Delay d) Cycle time

7. The minimum time delay between two successive memory read operations is _____
a) Cycle time b) Latency
c) Delay d) None of the mentioned

8. MFC is used to _____
a) Issue a read signal
b) Signal to the device that the memory read operation is complete
c) Signal the processor the memory operation is complete
d) Assign a device to perform the read operation

9. _____ is the bootleneck, when it comes computer performance.
a) Memory access time **b) Memory cycle time**
c) Delay d) Latency

10. The logical addresses generated by the cpu are mapped onto physical memory by _____
a) Relocation register b) TLB

c) MMU d) None of the mentioned

11. VLSI stands for _____
a) Very Large Scale Integration b) Very Large Stand-alone Integration
c) Volatile Layer System Interface d) None of the mentioned

12. The cells in a row are connected to a common line called _____
a) Work line **b) Word line**
c) Length line d) Principle diagonal
View Answer

13. The cells in each column are connected to _____
a) Word line b) Data line
c) Read line **d) Sense/ Write line**

14. The word line is driven by the _____
a) Chip select **b) Address decoder**
c) Data line d) Control line

15. 10. A 16 X 8 organisation of memory cells, can store upto _____
a) 256 bits b) 1024 bits
c) 512 bits **d) 128 bits**

16. A memory organisation that can hold upto 1024 bits and has a minimum of 10 address lines can be organised into _____
a) 128 X 8 b) 256 X 4
c) 512 X 2 **d) 1024 X 1**

17. Circuits that can hold their state as long as power is applied is _____
a) Dynamic memory **b) Static memory**
c) Register d) Cache

18. The number of external connections required in 16 X 8 memory organisation is _____
a) 14 b) 19 c) 15 d) 12

19. The advantage of CMOS SRAM over the transistor one's is _____
a) Low cost b) High efficiency
c) High durability **d) Low power consumption**

20. In a 4M-bit chip organisation has a total of 19 external connections.then it has _____ address if 8 data lines are there.
a) 10 b) 8 **c) 9** d) 12

Asynchronous DRAM

21. The Reason for the disregarding of the SRAM's is _____
a) Low Efficiency b) High power consumption
c) High Cost d) All of the mentioned

22. The disadvantage of DRAM over SRAM is/are _____
a) Lower data storage capacities b) Higher heat descipation
c) The cells are not static d) All of the mentioned

23. The reason for the cells to lose their state over time is
a) The lower voltage levels **b) Usage of capacitors to store the charge**
c) Use of Shift registers d) None of the mentioned

24. The capacitors lose the charge over time due to
a**) The leakage resistance of the capacitor**
b) The small current in the transistor after being turned on
c) The defect of the capacitor
d) None of the mentioned

25. _____ circuit is used to restore the capacitor value.
a) Sense amplify b) Signal amplifier
c) Delta modulator d) None of the mentioned

26. To reduce the number of external connections reqiured, we make use of _____
a) De-multiplexer **b) Multiplexer**
c) Encoder d) Decoder

27. The processor must take into account the delay in accessing the memory location, such memories are called _____
a) Delay integrated **b) Asynchronous memories**
c) Synchronous memories d) Isochronous memories

28. To get the row address of the required data _____ is enabled.
a) CAS **b) RAS** c) CS d) Sense/write

29. In order to read multiple bytes of a row at the same time, we make use of _____
a) Latch b) Shift register
c) Cache d) Memory extension

30. The block transfer capability of the DRAM is called _____
a) Burst mdoe b) Block mode
c) Fast page mode d) Fast frame mode

Synchronous DRAM

31. The difference between DRAM's and SDRAM's is/are _____
a) The DRAM's will not use the master slave relationship in data transfer
b) The SDRAM's make use of clock
c) The SDRAM's are more power efficient
d) None of the mentioned

32. The difference in address and data connection between DRAM's and SDRAM's is
a) The usage of more number of pins in SDRAM's
b) The requirement of more address lines in SDRAM's
c) The usage of buffer in SDRAM's
d) None of the mentioned

33. A _____ is used to restore the contents of the cells.
a) Sense amplifier **b) Refresh counter**
c) Restorer d) None of the mentioned

34. The mode register is used to
a) Select the row or column data transfer mode
b) Select the mode of operation
c) Select mode of storing the data
d) All of the mentioned

35. In a SDRAM each row is refreshed every 64ms.
a) True b) False

36. The time taken to transfer a word of data to or from the memory is called as _____

a) Access time b) Cycle time
c) Memory latency d) None of the mentioned

37. In SDRAM's buffers are used to store data that is read or written.

a) True b) False

38. The SDRAM performs operation on the _____

a) Rising edge of the clock b) Falling edge of the clock
c) Middle state of the clock d) Transition state of the clock

39. DDR SDRAM's perform faster data transfer by

a) Integrating the hardware **b) Transfering on both edges**
c) Improving the clock speeds d) Increasing the bandwidth

40. To improve the data retrieval rate

a) The memory is divided into two banks
b) The hardware is changed
c) The clock frequency is increased
d) None of the mentioned

Large memories

41. The chip can be disabled or cut off from external connection using _____

a) Chip select b) LOCK
c) ACPT d) RESET

42. To organise large memory chips we make use of _____

a) Integrated chips b) Upgraded hardware
c) Memory modules d) None of the mentioned

43. The less space consideration as lead to the development of _____ (for large memories).

a) SIMM's b) DIMS's c) SSRAM's **d) Both SIMM's and DIMS's**

44. The SRAM's are basically used as _____

a) Registers
b) Caches
c) TLB

d) Buffer

45. The higher order bits of the address are used to _____
a) Specify the row address
b) Specify the column address
c) Input the CS
d) None of the mentioned

46. The address lines multiplexing is done using _____
a) MMU
b) Memory controller unit
c) Page table
d) Overlay geberator

47. The controller multiplexes the addresses after getting the _____ signal.
a) INTR
b) ACK
c) RESET
d) Request

48. The RAS and CAS signals are provided by the _____
a) Mode register
b) CS
c) Memory controller
d) None of the mentioned

49. Consider a memory organised into 8K rows, and that it takes 4 cycles to complete a read opeartion. Then the refresh overhead of the chip is _____
a) 0.0021
b) 0.0038
c) 0.0064
d) 0.0128

50. When DRAM's are used to build a complex large memory,then the controller only provides the refresh counter.
a) True
b) False

Read-Only Memory

51. If the transistor gate is closed, then the ROM stores a value of 1.
    a) True
    b) False

52. PROM stands for _____
    a) Programmable Read Only Memory
    b) Pre-fed Read Only Memory
    c) Pre-required Read Only Memory
    d) Programmed Read Only Memory

53. The PROM is more effective than ROM chips in regard to _____
    a) Cost
    b) Memory management
    c) Speed of operation
    d) Both Cost and Speed of operation

54. The difference between the EPROM and ROM circuitry is _____
    a) The usage of MOSFET's over transistors
    b) The usage of JFET's over transistors
    c) The usage of an extra transistor
    d) None of the mentioned

55. The ROM chips are mainly used to store _____
    a) System files
    b) Root directories
    c) Boot files
    d) Driver files

56. The contents of the EPROM are erased by _____
    a) Overcharging the chip
    b) Exposing the chip to UV rays
    c) Exposing the chip to IR rays
    d) Discharging the Chip

57. The disadvantage of the EPROM chip is _____
    a) The high cost factor
    b) The low efficiency
    c) The low speed of operation
    d) The need to remove the chip physically to reprogram it

58. EEPROM stands for Electrically Erasable Programmable Read Only Memory.
a) True
b) False

59. The disadvantage of the EEPROM is/are _____
a) The requirement of different voltages to read,write and store information
b) The Latency inread operation
c) The inefficient memory mapping schemes used
d) All of the mentioned

60. The memory devices which are similar to EEPROM but differ in the cost effectiveness is _____
a) Memory sticks
b) Blue-ray devices
c) Flash memory
d) CMOS

61. The only difference between the EEPROM and flash memory is that the latter doesn't allow bulk data to be written.
a) True
b) False

62. The flash memories find application in _____
a) Super computers
b) Mainframe systems
c) Distributed systems
d) Portable devices

63. The memory module obtained by placing a number of flash chips for higher memory storage called as _____
a) FIMM
b) SIMM
c) Flash card
d) RIMM

64. The flash memory modules designed to replace the functioning of an harddisk is _____
a) RIMM
b) Flash drives
c) FIMM

d) DIMM

65. The reason for the fast operating speeds of the flash drives is
a) The absence of any movable parts
b) The itegarated electronic hardware
c) The improved bandwidth connection
d) All of the mentioned

Hierarchy of Memory

66. The standard SRAM chips are costly as _____
a) They use highly advanced micro-electronic devices
b) They house 6 transistor per chip
c) They require specially designed PCB's
d) None of the mentioned

67. The drawback of building a large memory with DRAM is _____
a) The large cost factor
b) The inefficient memory organisation
c) The Slow speed of operation
d) All of the mentioned

68. To overcome the slow operating speeds of the secondary memory we make use of faster flash drives.
a) True
b) False

69. The fastest data access is provided using _____
a) Caches
b) DRAM's
c) SRAM's
d) Registers

70. The memory which is used to store the copy of data or instructions stored in larger memories, inside the CPU is called _____
a) Level 1 cache
b) Level 2 cache
c) Registers
d) TLB

71. The larger memory placed between the primary cache and the memory is called _____
a) Level 1 cache
b) Level 2 cache
c) EEPROM
d) TLB

72. The next level of memory hierarchy after the L2 cache is _____
a) Secondary storage
b) TLB
c) Main memory
d) Register

73. The last on the hierarchy scale of memory devices is _____
a) Main memory
b) Secondary memory
c) TLB
d) Flash drives

74. In the memory hierarchy, as the speed of operation increases the memory size also increases.
a) True
b) False

75. If we use the flash drives instead of the harddisks, then the secondary storage can go above primary memory in the hierarchy.
a) True
b) False

Caches

76.The reason for the implementation of the cache memory is _____
a) To increase the internal memory of the system
b) The difference in speeds of operation of the processor and memory
c) To reduce the memory access and cycle time
d) All of the mentioned

77. The effectiveness of the cache memory is based on the property of _____
a) Locality of reference
b) Memory localisation
c) Memory size

d) None of the mentioned

78. The temporal aspect of the locality of reference means
a) That the recently executed instruction wont be executed soon
b) That the recently executed instruction is temporarily not referenced
c) That the recently executed instruction will be executed soon again
d) None of the mentioned

79. The spatial aspect of the locality of reference means
a) That the recently executed instruction is executed again next
b) That the recently executed wont be executed again
c) That the instruction executed will be executed at a later time
d) That the instruction in close proximity of the instruction executed will be executed in future

80. The correspondence between the main memory blocks and those in the cache is given by _____
a) Hash function
b) Mapping function
c) Locale function
d) Assign function

81. The algorithm to remove and place new contents into the cache is called _____
a**) Replacement algorithm**
b) Renewal algorithm
c) Updation
d) None of the mentioned

82. The write-through procedure is used
a) To write onto the memory directly
b) To write and read from memory simultaneously
c) To write directly on the memory and the cache simultaneously
d) None of the mentioned

83. The bit used to signify that the cache location is updated is _____
a) Dirty bit
b) Update bit
c) Reference bit
d) Flag bit

84. The copy-back protocol is used
a) To copy the contents of the memory onto the cache
b) To update the contents of the memory from the cache
c) To remove the contents of the cache and push it on to the memory
d) None of the mentioned

85. The approach where the memory contents are transferred directly to the processor from the memory is called _____
a) Read-later
b) Read-through
c) Early-start
d) None of the mentioned

Mapping Functions

86.The memory blocks are mapped on to the cache with the help of _____
a) Hash functions
b) Vectors
c) Mapping functions
d) None of the mentioned

87. During a write operation if the required block is not present in the cache then _____ occurs.
a) Write latency
b) Write hit
c) Write delay
d) Write miss

88. In _____ protocol the information is directly written into main memory.
a) Write through
b) Write back
c) Write first
d) None of the mentioned

89. The only drawback of using the early start protocol is _____
a) Time delay
b) Complexity of circuit
c) Latency
d) High miss rate

90. The method of mapping the consecutive memory blocks to consecutive cache blocks is called _____
a) Set associative
b) Associative
c) Direct
d) Indirect

91. While using the direct mapping technique, in a 16 bit system the higher order 5 bits is used for _____
a) Tag
b) Block
c) Word
d) Id

92. In direct mapping the presence of the block in memory is checked with the help of block field.
a) True
b) False

93. In associative mapping, in a 16 bit system the tag field has _____ bits.
a) 12
b) 8
c) 9
d) 10

94. The associative mapping is costlier than direct mapping.
a) True
b) False

95. The technique of searching for a block by going through all the tags is _____
a) Linear search
b) Binary search
c) Associative search
d) None of the mentioned

96. The set associative map technique is a combination of the direct and associative technique.
a) True

b) False

97. In set-associative technique, the blocks are grouped into _____ sets.
a) 4
b) 8
c) 12
d) 6

98. A control bit called ____ has to be provided to each blocj in set-associative.
a) Idol bit
b) Valid bit
c) Reference bit
d) All of the mentioned

99. The bit used to indicate whether the block was recently used or not is _____
a) Idol bit
b) Control bit
c) Reference bit
d) Dirty bit

100. Data which is not up-to date is called as _____
a) Spoilt data
b) Stale data
c) Dirty data
d) None of the mentioned

Cache Miss and Hit

101. The main memory is structured into modules each with its own address register called _____
a) ABR
b) TLB
c) PC
d) IR

102. When consecutive memory locations are accessed only one module is accessed at a time.
a) True
b) False

103. In memory interleaving, the lower order bits of the address is used to
a) Get the data
b) Get the address of the module
c) Get the address of the data within the module
d) None of the mentioned

104. The number successful accesses to memory stated as a fraction is called as _____
a) Hit rate
b) Miss rate
c) Success rate
d) Access rate

105. The number failed attempts to access memory, stated in the form of fraction is called as _____
a) Hit rate
b) Miss rate
c) Failure rate
d) Delay rate

106. In associative mapping during LRU, the counter of the new block is set to '0' and all the others are incremented by one,when _____ occurs.
a) Delay
b) Miss
c) Hit
d) Delayed hit

107. In LRU, the referenced blocks counter is set to'0' and that of the previous blocks are incremented by one and others remain same, in case of _____
a) Hit
b) Miss
c) Delay
d) None of the mentioned

108. If hit rates are well below 0.9, then they're called as speedy computers.
a) True
b) False

109. The extra time needed to bring the data into memory in case of a miss is called as _____
a) Delay
b) Propagation time

c) Miss penalty
d) None of the mentioned

110. The miss penalty can be reduced by improving the mechanisms for data transfer between the different levels of hierarchy.

a) True
b) False