LAKSHMI BARLA

D.No:18-88, FF – II, Salomi Residency, Adithya Nagar, Madhurawada,

Adithya Nagar, E-mail : blakshmi@gvpcew.ac.in

: lakshmibarla207@gmail.com

Visakhapatnam – 48. Mobile : +91-9493915870

Career Objective :

To work in a creative, challenging environment and achieve growth oriented career in an organization where I can contribute best to the growth of the organization and my technical skills.

Teaching Experience

- ♦ Currently working as Assistant Professor in Department of ECE in Gayatri Vidya Parishad College of Engineering for Women from August 2011 to till date.
- ♦ Worked as Assistant Professor in Department of Electronics & Communication Engineering, Viswanadha Institute of Technology and Management from July 2004 to October 2008.

Academic Record :

Qualification	School/College	University/Board	Period	Percentage of Marks
M.Tech (VLSI System Design)	St. Therissa college of Engineering, Garividi, Vizianagaram.	J.N.T.U,Kakinada	2008-2010	71
B.Tech (ECE)	SISTAM College of Engineering, Srikakulam	J.N.T.U,Kakinada	1999-2003	66
DIPLOMA (ECE)	Govt. Polytechnic Narsipatnam	State Board of Technical Education & Training	1995-1998	69
S.S.C	A.P. Residential School, Peddapuram, E.G	Board of Secondary Education, A.P.	1994-1995	75

Technical Skills:

◆ Languages : C, VHDL, Verilog

Software Packages : MATLAB and Mentor Graphics

Personality Traits:

- ♦ Ability to work in teams.
- ♦ Adaptability to new environments.
- Ability to work in time bound crisis situations.
- Hard working and result oriented.

Member Ship:

• Member of Indian Society for Technical Education.

Subjects Taught:

Digital IC Applications VLSI Design

Low power VLSI Design Electronic Devices & Circuits

Pulse & Digital Circuits Digital Logic Design

Linear Integrated Circuit Applications Digital System Design

Switching Theory and Logic Design Electronic Circuit Analysis

Analog Communications Digital Communications

CMOS Mixed Signal Circuit Design

CMOS Analog IC Design

Design of Fault Tolerant Systems

Signals & Systems

Online Courses (NPTEL):

S.No.	Title of Lecture	Organization	Duration & Dates	Score
		Details		
			12 WEEKS	81%
1	ANALOG CIRCUITS	NPTEL	31/01/2018 -	
			21/04/2018	
			12 WEEKS (JULY-	80%
2	DIGITAL CIRCUITS	NPTEL	OCT,2018)	
			12 WEERS (IIII V	86%
3	MICROELECTRONICS:DEVICES TO CIRCUITS	NPTEL	12 WEEKS (JULY- OCT,2019)	00%

Conferences & Publications:

- ♦ B Lakshmi, M Kama Raju, K Babulu "Subthreshold Region based Linear Feedback Shift Register" International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 8958, Volume-8, Issue-6S2, August 2019.
- ♦ B Lakshmi, Dr. M Kama Raju, Dr. K Babulu "Design and implementation of Linear Feedback Shift Register in Subthreshold Region" International Conference on Computational and Intelligent Techniques for Automation of Engineering.
- ♦ K.Venkata laxmi, B.Lakshmi" Power Efficient and Noise Immune Domino Logic for Wide Fan in Gates"(IJAEEIE)International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 3, Issue 10, October 2014

FDP's & Workshops:

- A One and Half week FDP on "Microelectronics:Devices To Circuits", Organized by the IIT Roorkee.
- A two week summer FDP on Important Engineering Subjects, Organized by the JNTUK Kakinada .2019.
- A three day National workshop on "Cryptology and Cyber Security", GVPCEW, 2018.

- A three day workshop on "Custom Analog and Digital IC Design using Mentor EDA Tools", GVPCEW, 2018.
- A Two- week ISTE STTP on "CMOS, Mixed Signal and Radio frequency VLSI Design" Conducted by Indian Institute of Technology Kharagpur, 2017.
- A Two day Workshop on "Signal Processing and Communication Systems" Organized by the GVPCEW,2017.
- Workshop on "EMRF" conducted at Gayatri Vidya Parishad College of Engineering for Women in 2016.
- Workshop on "Cognitive Radio Technologies" conducted at Gayatri Vidya Parishad College of Engineering for Women in 2015.
- Workshop on "VLSI & EDA Tools" conducted at JNTU-Vizianagram in 2013.
- Workshop on "System Design Using XILINX FPGA?s" conducted at Gayatri Vidya Parishad College of Enggineering in 2011.
- Workshop on "VLSI & Embedded Systems" conducted at Viswanadha Institute of Technology and Management in 2009.
- Workshop on "Signal processing Evolutionary computational and modelling" conducted at DIETCE, Anakapalli in 2009.
- Workshop on "Recent Developments in information & Communications Technologies" conducted at AITAMCE, Tekkali in 2008.

Personal Profile:

Date of birth : 05 - 12 - 1978

Father's name : B Appala Naidu

Gender : Female

Marital status : Married

Languages known : English and Telugu

Nationality : Indian.

Declaration:

I here by declare that all the information mentioned above is true to the best of my knowledge.

Date:	
Place:	[BARLA LAKSHMI]