

About The Institution

G.V.P. College of Engineering for Women is established under the aegis of Gayatri Vidya Parishad, an educational society founded by eminent academicians, industrialists, and Philanthropists of Visakhapatnam. To empower women in technological and engineering fields, the society has established this engineering college exclusively for women in the year 2008. It is a self-financed institution offering excellence in engineering education and is affiliated to Jawaharlal Nehru Technological University, Kakinada (JNTUK), approved by AICTE, New Delhi.

The College is offering UG courses in ECE, EEE, CSE, IT and a PG Course in ECE. The institute has very good infrastructural facilities, e-classrooms, and well equipped laboratories. The college has well qualified faculty to train the women engineers who are in pursuit of their professional careers in the courses offered by the institute.

About Department Of ECE

The department of Electronics and Communication Engineering offers B.Tech Program in E.C.E and M.Tech program in VLSI Design and Embedded Systems. The department has a team of 23 dedicated and experienced faculty members out of which 4 faculty hold Ph.D degree. The department has state-of-the-art laboratories with advanced software and hardware to facilitate research in major areas of ECE. The ECE department started in 2008 with an initial intake of 120 students in UG Program. In 2011, the department started a PG Program in VLSI Design & Embedded Systems with an intake of 18 students.

About CoreEL Tehnologies

CoreEL Technologies is a Customer Application Specific Product & Solutions (CASPS) company offering innovative solutions, ranging across Intellectual Property (IP) cores, Design & Development, -System Design & Prototype Development, Next-Gen Digital products, Integrated solutions, Low Volume Manufacturing, System Upgrades and Obsolescence management, EDA tools, COTS products, Semiconductor solutions and Technology Training. They are a leading developer of advanced electronic system level products and solutions.

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Assoc. Professor and HOD, E.C.E.

Organizing Secretaries

Mrs. Ch. Sirisha, *Asst. Professor, E.C.E*

Mrs. M. Mani Kumari, *Asst. Professor, E.C.E*

MAILING ADDRESS

All the correspondence may be addressed to

Mrs. Ch. Sirisha, Asst. Professor, ECE,
Mobile: 9849550004

E-mail: chsirisha216@gvpcew.ac.in



Custom Analog & Digital IC Design Using Mentor EDA Tools (ADICD -2018)

27th, 28th & 29th September, 2018

Organized by

**Department of Electronics and Communication Engineering
Gayatri Vidya Parishad
College of Engineering for Women**

In Technical association with



Enabling Excellence

**CoreEL Technologies (I) Pvt. Ltd.,
Bangalore**

**Gayatri Vidya Parishad
College of Engineering for Women
Madhurawada, Visakhapatnam - 530 048
Phone: 0891-2739144; Fax: 0891-2526639
Visit us at: www.gvpcew.ac.in**

Objective Of The Workshop

The aim of this workshop is to provide hands-on experience on the state-of-the-art Mentor EDA tools for VLSI Design to enhance practical skills and knowledge to solve real world technical problems. The participants will have an exposure to the Circuit Design & Simulation, Layout Generation, Physical Design and Verification, and Parasitic Extraction.

Detailed Areas of Focus

- ✓ Full Custom Design flow
 - ❖ Mentor Tool for Schematic and layout generation
 - ❖ DRC (Design rule check) and LVS checking
 - ❖ Parasitic Extraction
 - ❖ Configuration of the design using FPGA Protoboards using Xilinx ISE tool
- ✓ Analog Design Flow
 - ❖ AC, DC and Transient Analysis
 - ❖ Layout Entry for CS/ Differential Amplifier
- ✓ Semi Custom Design Flow
 - ❖ Verilog Entry
 - ❖ Layout design from Verilog netlist
 - ❖ Physical Design and Verification
- ✓ Cell based Design

Resource Persons

Prof. Dr. N.Balaji,

HOD (ECE) & Vice-Principal (Admn.),
UCEN, JNTU, Narasaraopet, Guntur.

Mr. Nagendra Bandi,

Senior Application Engineer,
CoreEL Technologies (I) Pvt Ltd, Bangalore.

Mr. Rajesh Murugan,

Application Engineer,
CoreEL Technologies (I) Pvt Ltd, Bangalore.

Organizing Committee

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Mr. K.S.A. Naidu, Asst.Prof, E.C.E

Mr. P.V. Dileep Bhumireddy, Asst.Prof, E.C.E

Registration

PG students & Research Scholars	Rs. 400/-
For Faculty	Rs. 500/-
For Industrial Delegates	Rs. 750/-

A photo copy of the accompanying registration form, duly filled, should be sent along with a DD drawn in favor of Principal, GVPCEW, payable at Visakhapatnam.

Registration fee include workshop kit, lunch and refreshments during the workshop only.

Who Can Participate

- ✓ UG students working in area of VLSI design
- ✓ Researchers (Masters, Doctoral students and Fellows) with thesis in VLSI
- ✓ Academicians for enhancing skills in delivering VLSI Labs at Institute/University
- ✓ Design engineers from industry

Last Date for registration : 21st Sept, 2018

A THREE DAY WORKSHOP

On

Custom Analog & Digital IC Design Using Mentor EDA Tools (ADICD -2018)

27th, 28th & 29th September, 2018

REGISTRATION FORM

Participant's Name :

Qualification :

Department :

Institution/Organization:

Address for Communication:

Phone No (O): (R):

E-mail ID :

Registration Fee :

D.D No. Date:

Name of the Bank:

Accommodation is required: YES / NO

Date:

Signature of the Participant

SPONSORSHIP CERTIFICATE

Mr./Ms. _____ is sponsored to attend the Workshop on "Custom Analog & Digital IC Design Using Mentor EDA Tools (ADICD-18)", from 27th to 29th September, 2018.

Place:

Date:

Signature of the Head of the Department/Institution with Seal